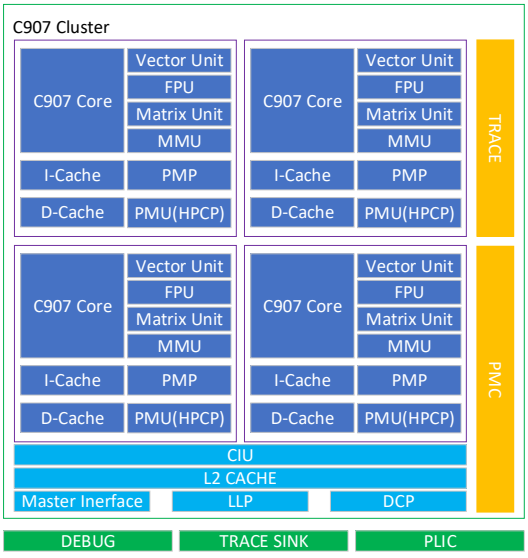
XUANTIE 玄铁

Full support with Vector1.0 and XuanTie Matrix

XuanTie C907 Datasheet



Overview

C907 is a RISC-V compatible 64-bit power efficient processor with vector and matrix computation unit. It is based on the RV64GCB[V] and RV32GCB[V] instruction set, and compatible to RVB23 Profile.

C907 adopts a state of the art 9 stages in-order dual issue superscalar pipeline with a 128-bit vector unit implementing the RISC-V V Extension Version 1.0 .

C907 supports hardware cache coherency, containing 1-4 cores in each cluster. C907 supports the AXI4/ACE bus interface and includes two optional ports: A Device Coherence Port (DCP) for maintaining data coherency with external I/O masters and a Low Latency Port (LLP) for accessing peripherals.

C907 supports Sv32/Sv39/Sv48 virtual address system with Svnapot, Svpbmt. In addition, C907 includes the standard CLINT and PLIC interrupt controllers and supports RV-compatible debug interface, Nexus Trace and performance monitors.

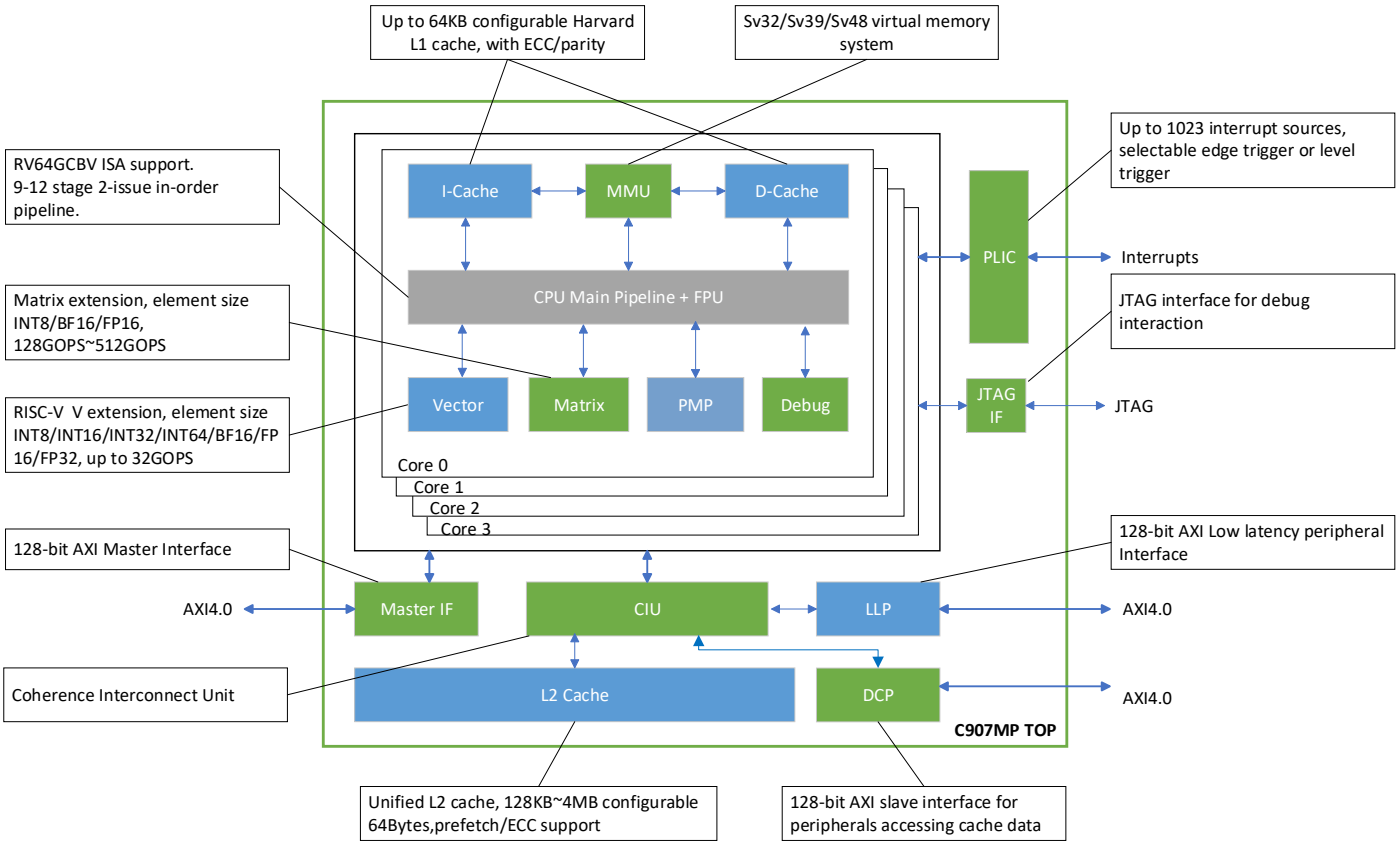
Application areas: Smart vision, sweeping robots, medical imaging, industrial vision, mobile internet, smart interactions (attendance machines, smart access control etc).

Features

Feature	Description
Architecture	RV64GCB[V]，RV32GCB[V]
SMP	Up to 4 cores in each cluster
Micro-architecture	In-order dual issue
Pipeline	9 stages (Integer)
Floating-Point Unit	Support RISC-V H, F and D instruction extensions Support IEEE 754-2008 standard
Vector Unit	Support RISC-V V extension
Bus Interface	AXI4 128-bit master
Device Coherence Port (DCP)	AXI4-128 slave (Optional)
Low Latency Port (LLP)	AXI4-128 master (Optional)
L1 Instruction Cache	Up to 64KB with optional parity
L1 Data Cache	Up to 64KB with optional ECC
L2 Cache	Up to 4MB with optional ECC supporting parallel access with multi-bank
XuanTie Extensions	XuanTie Instruction Extension (XIE)
MMU	Sv32/Sv39/Sv48 virtual memory translation along with Svnapot and Svpbmt
PMP	Up to 64 regions, ePMP
Interrupt Controller	Flexibly configurable Platform-Level Interrupt Controller (PLIC) for supporting wide range of system event scenarios
TEE	Support TEE extension
Matrix Unit	Support Matrix extension

XuanTie C907 Components

Processor Overview



Core

- ✧ Integer pipeline of 9 stages
- ✧ In-order dual-issue
- ✧ Various branch prediction resources (Branch History Table, Branch Target Buffer, Return Address Stack etc.)

Multi-Core and Multi-Cluster

- ✧ Support 1-4 core homogeneous multi-core and multi-cluster system
- ✧ MESI coherency protocol
- ✧ Inclusive and exclusive cache strategy
- ✧ Integrates multi-core interrupt controllers, timers, and debug modules

Floating Point Unit (FPU)

- ✧ RISC-V H, F and D extensions
- ✧ Support half/single/double precision
- ✧ Fully IEEE-754 compliant
- ✧ User configurable rounding modes

Vector Unit

- ✧ RISC-V V Extension (Version 1.0)
- ✧ Support 128/256-bit VGPR
- ✧ Support element size of INT8/INT16/INT32/INT64/BF16/FP16/FP32
- ✧ Vector chaining technology to enhance computing throughput
- ✧ Segment load/store supported
- ✧ D-Cache data path width up to 128 bits
- ✧ Unaligned memory access acceleration

Memory sub-system

The L1 caches in C907 can be configured as 16KB/32KB/64KB. The four cores in a cluster share an L2 cache with a configurable size of 128KB~4MB. Data coherency is maintained by hardware among all the L1 and L2 caches. Furthermore, data coherency between TLB, I-Cache and D-Cache is maintained by software and hardware collaboration. The L1 and L2 caches support ECC/parity.

- ✧ The L1 instruction memory system has the following key features:
  - • VIPT, four-way set-associative instruction cache
  - • Optional parity protection
  - • Fixed cache line length of 64 bytes
- ✧ The L1 data memory system has the following features:
  - • VIPT, two-way set associative L1 data cache
  - • Optional ECC protection
  - • Fixed cache line length of 64 bytes
  - • Up to 128-bit read data paths from the data L1 memory system to the data path
  - • Up to 128-bit write data path from the data path to the L1 memory system
- ✧ The L2 Cache has the following features:
  - • Configurable size of 128KB, 256KB, 512KB, 1MB, 1.5MB, 2MB, 3MB, or 4MB
  - • PIPT, 16-way set-associative structure
  - • Fixed line length of 64 bytes
  - • Optional ECC protection

• Support data prefetch

Memory Management Unit (MMU)

- ✧ Sv32/Sv39/Sv48 virtual memory systems supported with 32-bit or 40-bit physical address
- ✧ 16/16-entry fully associative I-uTLB/D-uTLB
- ✧ 256/512-entry 2-way set-associative shared TLB
- ✧ Hardware page table walker
- ✧ Virtual memory support for full address space and easy hardware for fast address translation
- ✧ Code/data sharing
- ✧ Support for full-featured OS such as Linux

Physical Memory Protection (PMP)

- ✧ Up to 64 regions read/write/execute memory protection with low cost
- ✧ Support OFF, TOR and NAPOT
- ✧ Optional EPMP

Platform-Level Interrupt Controller (PLIC)

- ✧ Support multi-core, multi-cluster interrupt control
- ✧ Up to 1023 PLIC interrupt sources
- ✧ Up to 32 PLIC interrupt priority levels
- ✧ Up to 256 PLIC interrupt targets
- ✧ Selectable edge trigger or level trigger

JTAG Debug

- ✧ RISC-V debug
- ✧ Support multi-core debug
- ✧ JTAG debug interface support several triggers
- ✧ Support software breakpoints
- ✧ Check and modify CPU register resource
- ✧ Single step or multi step flexibly supported
- ✧ High speed program download through JTAG

Low Power

- ✧ Support WFI instruction and WRS instruction for low power mode

- ✧ Sub-module clocks are gated automatically when they are idle
- ✧ Multiple Power Domains
- ✧ IPMC for power mode control

Security

- ✧ Up to 16 zones
- ✧ Secure boot
- ✧ Isolation between TEE and REE
- ✧ Isolation between TA (Trusted Application) and TEE
- ✧ Isolation between TA and TA
- ✧ Support ePMP and TEE for PMP
- ✧ Support TEE for TLB, Debug and PLIC

XuanTie Extensions

In addition to the standard RV64GCB[V] ISA, C907 has also implemented the XIE (XuanTie Instruction Extension). The XIE consists of extended instructions optimized for load/store, arithmetic, bitwise and cache/TLB operations. When enabled, these instructions improve the performance significantly.

RV Compatibility

- ✧ Compatible to RVB23 Profile

Interfaces

- ✧ Master AXI (M-AXI)
- ✧ DCP (S-AXI)
- ✧ LLP (M-AXI)
- ✧ Debug (JTAG)
- ✧ Interrupts
- ✧ Low power control

PPA

Performance	2.98 DMIPS/MHz 3.93 Coremark/MHz
Frequency	1.2^{1} ~ 1.35^{2}GHz
Area	0.7^{1} ~1.1^{2} mm^{2} Per Core

Power	Leakage 22.4[1] ~ 38.2[2]mW per Core
	Dynamic 76.4[1] ~ 102[2]mW/GHz per Core
1. Efficiency config: 32K icache + 32K dcache + Vector + FP 2. Performance config: 32K icache + 32K dcache + Vector + FP + Matrix TSMC 28HPCP 9T LVT+SVT+HVT 30p+35p+40p (Efficiency w.o. 30plvt) Implemented by FusionCompiler to PostRoute stage Frequency@ssg0p81vm40c; Power@tt0p9v85c	

Configurations

Config	Options
Core Number	1-4
L1 D-Cache Size	16K, 32K, 64K
L1 I-Cache Size	16K, 32K, 64K
L2-Cache Size	128K, 256K, 512K, 1M, 1.5M, 2M, 3M, 4M
Vector Unit	Present or not
DCP	Present or not
LLP	Present or not
Matrix Unit	No, Min, Standard, Max

Software Ecosystems

Application Scenarios	Linux Distributions: yocto PROJECT ... Multimedia Applications: ffmpeg/gstreamer/Webserver(thttpd)/RTSP/RTMP/Onvif/... Container: docker ...
Libraries	OpenBlas, OpenCV, OpenGL, OpenCL, OpenVG, OpenSSL ...
OS Kernel	Linux freeRTOS RT-Thread ...
Development Languages	C C++ python ...
Debug Tools	Open On-Chip Debugger SEGGER LAUTERBACH DEVELOPMENT TOOLS CSkyDebugServer CKLink Lite CKLink Pro ...
Development Tools	GCC LLVM IAR SYSTEMS QEMU ...