XuanTie C Series Processor Comparison Table

The XuanTie C series is designed for high performance, AI enhancement, and versatile application scenarios. These processors are suitable for various fields including PCs, servers, autonomous driving, AI inference, edge computing, AR/VR, smart interaction, consumer electronics, etc.

For more details, see individual C series processor product page.

Feature	C906	C907	C908	C908X	C910	C920	C930
Architecture	RV64IMA[FD]C[V]	RV64GCB[V], RV32GCB[V]	RV64GCB[V]	RV64GCB[V]	RV64GC	RV64GC[V]	RVA23 Profile
SMP	/	Up to 4 cores per cluster	Up to 4 cores per cluster	Up to 4 cores per cluster	Up to 4 cores per cluster	Up to 4 cores per cluster	Up to 8 cores per cluster with XT-Link
Pipeline Stage (Integer)	5	9	9	9	12	12	16
XuanTie Extensions	XuanTie Instruction Extension (XIE) XuanTie Memory Attribute Extension (XMAE)	XuanTie Instruction Extensions (XIE) XuanTie Matrix Extension（MME）	XuanTie Instruction Extension (XIE) XuanTie Memory Attribute Extension (XMAE)	XuanTie Instruction Extension (XIE) XuanTie Memory Attribute Extension (XMAE)	XuanTie Instruction Extension (XIE) XuanTie Memory Attribute Extension (XMAE)	XuanTie Instruction Extension (XIE)	XuanTie Instruction Extension (XIE)
Floating-Point Unit	RV F/D instructions (optional)	RV F/D instructions (optional)	RV F/D instructions	RV F/D instructions	RV F/D instructions	RV F/D instructions	RV Zfh, Zfhmin, Zfbfmin, F, D instructions
Vector Unit	Optional, VLEN 128	Optional, VLEN 128/256	Optional, VLEN 128/256	VLEN 512/1024/4096	/	Optional, VLEN 128 Supports unaligned access	VLEN 256 Supports unaligned access
Master Device Interface	AMBA4 AXI4	AMBA4 ACE or AXI4	AMBA4 ACE or AXI4	AMBA4 ACE or AXI4	AMBA4 AXI4	AMBA4 ACE or AXI4	Direct connection mode: CHI.E/CHI.F Non-direct connection mode: AMBA4 ACE or AXI4
Low-Latency Peripheral Port	/	AMBA4 AXI4	AMBA4 AXI4	AMBA4 AXI4	/	AMBA4 AXI4	AMBA4 AXI4
Device Coherence Port	/	ACE-LiteDVM or AXI4	AMBA4 AXI4	AMBA4 AXI4	AMBA4 AXI4	AMBA4 AXI4	AMBA ACE4-LiteDVM

Feature	C906	C907	C908	C908X	C910	C920	C930
L1 I-Cache	Up to 64KB	Up to 64KB, with optional parity check	Up to 64KB, with optional parity check	Up to 64KB, with optional parity check	Up to 64 KB, with optional parity check	Up to 64KB, with optional parity check	Typical configuration: 64KB; parity check (optional)
L1 D-Cache	Up to 64KB	Up to 64KB, with optional ECC check	Up to 64KB, with optional parity/ECC check	Up to 64KB, with optional parity/ECC check	Up to 64 KB, with optional ECC check	Up to 64KB, with optional ECC support	Typical configuration: 64KB; ECC check (optional)
L2 Cache	/	Up to 4MB, with optional ECC, supports multi-bank parallel access	Up to 4MB, with optional ECC check	Up to 4MB, with optional ECC check	Up to 8MB with optional ECC check	Up to 8MB, with optional ECC support	Typical configuration: 1MB; ECC check (optional)
Memory Management Unit	Sv39	Sv32/Sv39/Sv48, supporting Svnapot and Svpbmt extensions	Sv32/Sv39/Sv48, supporting Svnapot and Svpbmt extensions	Sv39/Sv48	Sv39	Sv39/Sv48, supporting Svnapot and Svpbmt extensions	Sv39/Sv48, supporting Svnapot and Svpbmt extensions
Physical Memory Protection	Up to 16 regions	Up to 64 regions with ePMP	Up to 64 regions with ePMP	Up to 64 regions with ePMP	Up to 16 regions	Up to 16 regions	Typical configuration: 16 regions
Coprocessor	/	/	/	Yes	/	Yes	Yes
Interrupt Controller	CLINT and PLIC	CLINT and PLIC with multi-cluster interrupt	CLINT and PLIC with multi-cluster interrupt	CLINT and PLIC with multi-cluster interrupt	CLINT and PLIC with multi-cluster interrupt	CLINT and PLIC with multi-cluster interrupt	Supports AIA 1.0
RISC-V Debug	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hardware Perfromance Monitoring	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Branch Prediction	BHT/BTB/RAS/etc.	BHT/BTB/RAS/etc.	BHT/BTB/RAS/etc.	BHT/BTB/RAS/etc.	BHT/BTB/RAS/etc.	BHT/BTB/RAS/etc.	BHT/BTB/RAS/etc.
Security	/	Support XuanTie TEE extension	Support XuanTie TEE extension	Support XuanTie TEE extension	Support XuanTie TEE extension	Support XuanTie TEE extension	Supports CFI/Smmtt/CoVE
DMIPS/MHz	2.3	2.98	3.82	4.1	5.8	6.2	/
CoreMark/MHz	3.7	3.93	5.71	5.7	6.96	7.2	/

XUANTIE

XuanTie, under Alibaba DAMO Academy, is committed to the continuous exploration of cutting-edge technological innovations and the construction of an open-source ecosystem for the RISC-V architecture. Our mission is to provide powerful, intelligent, secure, and open new computing architectures and reliable IP for the digital era.