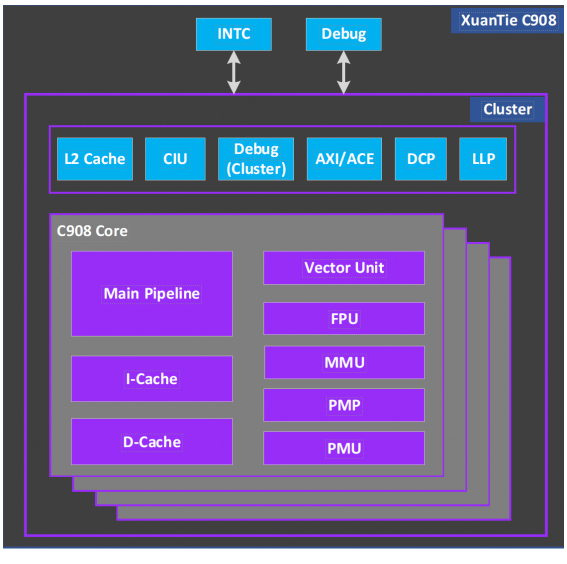
XUANTIE 玄铁

The world's first CPU to pass the RVA22

XuanTie C908 Datasheet

Overview



C908 is a RISC-V compatible 64-bit high performance processor with vector computing ability, developed by C-SKY MicroSystems Co., Ltd. It delivers industry-leading performance in control flow, computing and frequency through architecture and micro-architecture innovations.

The C908 processor is based on the RV64GCB[V] instruction set, compatible to RVA22 Profile and implements the XIE (XuanTie Instruction Extension) technology.

C908 adopts a state of the art 9 stages in order dual issue superscalar pipeline with high frequency, IPC, and power efficiency, with a 128-bit vector unit implementing the RISC-V V Extension Version 1.0 .

C908 supports hardware cache coherency. Each cluster contains 1-4 cores. The C908 supports the AXI4/ACE bus interface and includes two optional ports: A Device Coherence Port (DCP) for maintaining data coherency with external I/O masters and a Low Latency Port (LLP) for accessing peripherals.

The C908 supports the Sv39/Sv48 virtual address system with Svnapot, Svpbmt and XMAE (XuanTie Memory Attributes Extension) technology.

In addition, C908 includes the standard CLINT and PLIC interrupt controllers and supports RV-compatible debug interface and performance monitors.

C908 is a CPU core developed by XuanTie to meet the increasing needs of image and video processing in the IoT market.

Application areas: smart vision, intelligent interaction, HMI, AR/VR, 5G and other applications with requirements for power-efficiency.

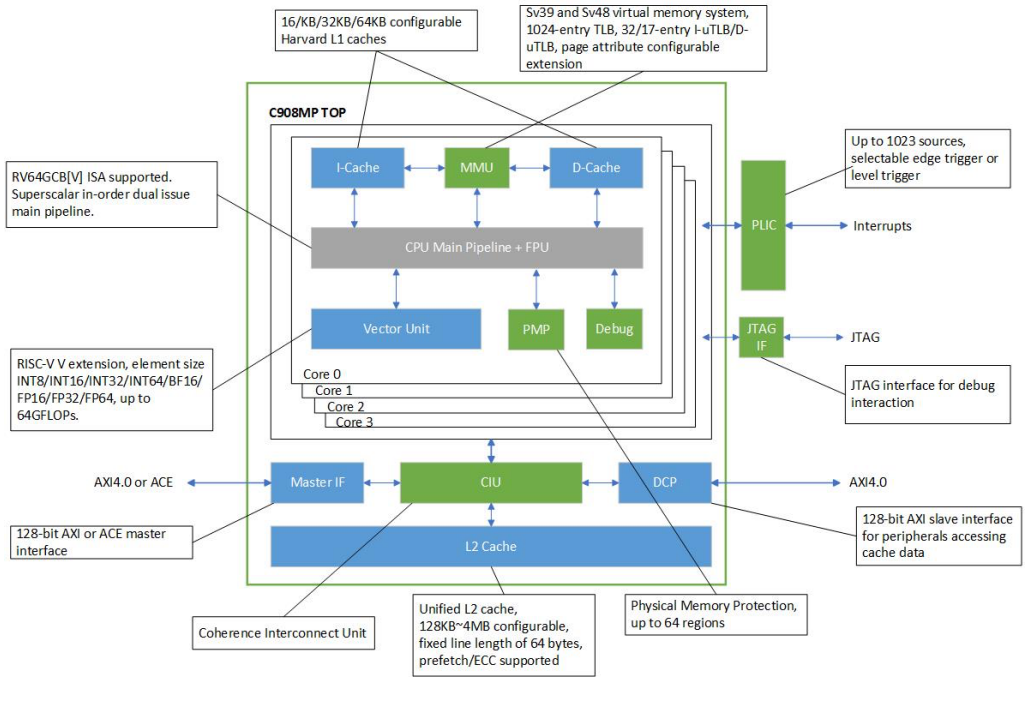
Additional application areas include sweeping robots, drones, automatic driving, AR, medical imaging, industrial vision, mobile internet etc.

Features

Feature	Description
Architecture	M/S mode: RV64GCB[V] U mode: RV64GCB[V]/ RV32GCB[V]
SMP	Up to 4 cores in each cluster
Micro-architecture	In-order dual issue
Pipeline	9 stages (Integer)
Floating-Point Unit	Support RISC-V H, F and D instruction extensions Support IEEE 754-2008 standard
Vector Unit	RISC-V V extension
Bus Interface	AXI4 or ACE 128-bit master
Device Coherence Port (DCP)	AXI4-128 slave (Optional)
Low Latency Port (LLP)	AXI4-128 master (Optional)
L1 Instruction Cache	Up to 64KB with optional parity
L1 Data Cache	Up to 64KB with optional ECC
L2 Cache	Up to 4MB with optional ECC supporting parallel access with multi-bank
XuanTie Extensions	XuanTie Instruction Extension (XIE) XuanTie Memory Attributes Extension (XMAE)
MMU	Sv39/Sv48 virtual memory translation along with Svnapot and Svpbmt
PMP	Up to 64 regions, ePMP
Interrupt Controller	Flexibly configurable Platform-Level Interrupt Controller (PLIC) for supporting wide range of system event scenarios
TEE	Support XuanTie TEE extension

XuanTie C908 Components

- **Processor Overview**



• Core

◇ Integer pipeline of 9 stages
◇ In-order dual-issue
◇ Various branch prediction resources (Branch History Table, Branch Target Buffer, Return Address Stack etc.) for high performance

• Multi-Core and Multi-Cluster

◇ Support 2-4 core homogeneous multi-core and multi-cluster system
◇ MOESI coherency protocol
◇ 2-way centralized snoop buffer
◇ Exclusive memory access instructions
◇ Integrates multi-core interrupt controllers, timers, and debug modules

• Floating Point Unit (FPU)

◇ RISC-V H, F and D extensions
◇ Support half/single/double precision
◇ Fully IEEE-754 compliant
◇ Does not generate floating-point exceptions
◇ User configurable rounding modes

• Vector Unit

◇ RISC-V V Extension (Version 1.0)
◇ Support 128/256-bit VGPR
◇ Support element size of INT8/INT16/INT32/
◇ INT64/BF16/FP16/FP32
◇ Vector chaining technology to enhance computing throughput
◇ Segment load/store supported
◇ D-Cache data path width up to 128 bits
◇ Unaligned memory access acceleration

• Memory sub-system

The L1 caches in C908 can be configured as 16KB/32KB/64KB. The four cores in a cluster share an L2 cache with a configurable size of 128KB~4MB. Data coherency is maintained by hardware among all the L1 and L2 caches. Furthermore, data coherency between TLB, I-Cache and D-Cache is maintained by software and hardware collaboration. The L1 and L2 caches support ECC/parity.

◇ The L1 instruction memory system has the following key features:

- VIPT, four-way set-associative instruction cache
- Optional parity protection
- Fixed cache line length of 64 bytes
- 128-bit read interface from the L2 memory system

◇ The L1 data memory system has the following features:

- PIPT, two-way set associative L1 data cache
- Fixed cache line length of 64 bytes
- Optional ECC protection
- 128-bit read interface from the L2 memory system
- Up to 128-bit read data paths from the data L1 memory system to the data path
- Up to 128-bit write data path from the data path to the L1 memory system

◇ The L2 Cache has the following features:

- Configurable size of 128KB, 256KB, 512KB, 1MB, 1.5MB, 2MB, 3MB, or 4MB
- PIPT, 16-way set-associative structure
- Fixed line length of 64 bytes
- Optional ECC protection
- Support data prefetch

Memory Management Unit (MMU)

- ◇ Sv39/Sv48 virtual memory systems supported with 40-bit physical address
- ◇ 16/16-entry fully associative I-uTLB/D-uTLB
- ◇ 512/1024-entry 4-way set-associative shared TLB
- ◇ Hardware page table walker
- ◇ Virtual memory support for full address space and easy hardware for fast address translation
- ◇ Code/data sharing
- ◇ Support for full-featured OS such as Linux
- ◇ XMAE (XuanTie Memory Attributes Extension) technology extends page table entries for additional attributes

Physical Memory Protection (PMP)

- ◇ Up to 64 regions read/write/execute memory protection with low cost

JTAG Debug

- ◇ RISC-V debug
- ◇ Support multi-core debug
- ◇ JTAG debug interface support several triggers
- ◇ Support software breakpoints
- ◇ Check and modify CPU register resource
- ◇ Single step or multi step flexibly supported
- ◇ High speed program download through JTAG

Platform-Level Interrupt Controller (PLIC)

- ◇ Support multi-core, multi-cluster interrupt control
- ◇ Up to 1023 PLIC interrupt sources
- ◇ Up to 32 PLIC interrupt priority levels
- ◇ Up to 256 PLIC interrupt targets
- ◇ Selectable edge trigger or level trigger

Low Power

- ◇ WFI instruction puts a core into low power mode
- ◇ Sub-module clocks are gated automatically when they are idle
- ◇ Per-core power down
- ◇ Cluster power down

Security

C908 supports the following security features:

- ◇ Up to 16 zones
- ◇ Secure boot
- ◇ Isolation between TEE and REE
- ◇ Isolation between TA (Trusted Application) and TEE
- ◇ Isolation between TA and TA
- ◇ Support ePMP and TEE for PMP
- ◇ Support TEE for TLB, Debug and PLIC

XuanTie Extensions

In addition to the standard RV64GCB[V] ISA, C908 has also implemented the XIE (XuanTie Instruction Extension). The XIE consists of extended instructions optimized for load/store, arithmetic, bitwise and cache/TLB operations. When enabled, these instructions improve the performance significantly. For example, the extended arithmetic instructions can achieve 40% better Coremark result.

RV Compatibility

Compatible to RVA22 Profile.

Interfaces

- ◇ Master AXI (M-AXI) or ACE
- ◇ DCP (S-AXI)
- ◇ LLP (M-AXI)
- ◇ Debug (JTAG)
- ◇ Interrupts
- ◇ Low power control

PPA

Performance	3.82 DMIPS/MHz 5.71 Coremark/MHz
Frequency	1.2[1] ~ 2[2]GHz (Typical)
Area	0.39[1] ~ 0.46[2] mm² per Core
Power	Leakage 8.9[1] ~ 24.6[2]mW per Core
	Dynamic 52.8[1] ~ 64.4[2]mW/GHz per Core

1.Low Power
2.High Performance
TSMC 12FFC 6-tracks Turbo uLVT-C16+uLVT-C20+uLVT-C24
Dynamic power@ tt0p8v85c, Frequency@ ssgnp0p72vm40c;
Configuration: MP4, 32K L1$, 1MB L2$, VLEN128, No ECC

Configurations

Config	Options
Core Number	1-4
L1 D-Cache Size	16K, 32K, 64K
L1 I-Cache Size	16K, 32K, 64K
L2-Cache Size	128K, 256K, 512K, 1M, 1.5M, 2M, 3M, 4M
Vector Unit	Present or not
DCP	Present or not
LLP	Present or not

Software Ecosystems

Application Scenarios	Linux Distributions: yocto PROJECT ... Multimedia Applications: ffmpeg/gstreamer/Webserver(thttpd)/RTSP/RTMP/Onvif/... Container: docker ...
Libraries	OpenBlas, OpenCV, OpenGL, OpenCL, OpenVG, OpenSSL ...
OS Kernel	Linux freeRTOS RT-Thread
Development Languages	C C++ python ...
Debug Tools	Open On-Chip Debugger CSkyDebugServer CKLink Lite CKLink Pro Third-party debugging tools
Development Tools	GCC LLVM IAR SYSTEMS QEMU